

# AMC-CAN4

## 4 Channel AMC CAN Module

- **Cost effective:** 4 channels onboard
- **High performance:** local data management by FPGA and bus mastering
- **Wide software support:** drivers for Windows, Linux, QNX and other operating systems

### AMC CAN Interfaces

The AMC-CAN4 features four CAN High-Speed interfaces according to ISO 11898-2. The CAN interfaces are electrically isolated against the controller potential and against each other. CAN status is displayed by two LEDs for each CAN channel placed at the RJ45 connectors.

### CAN Data Management

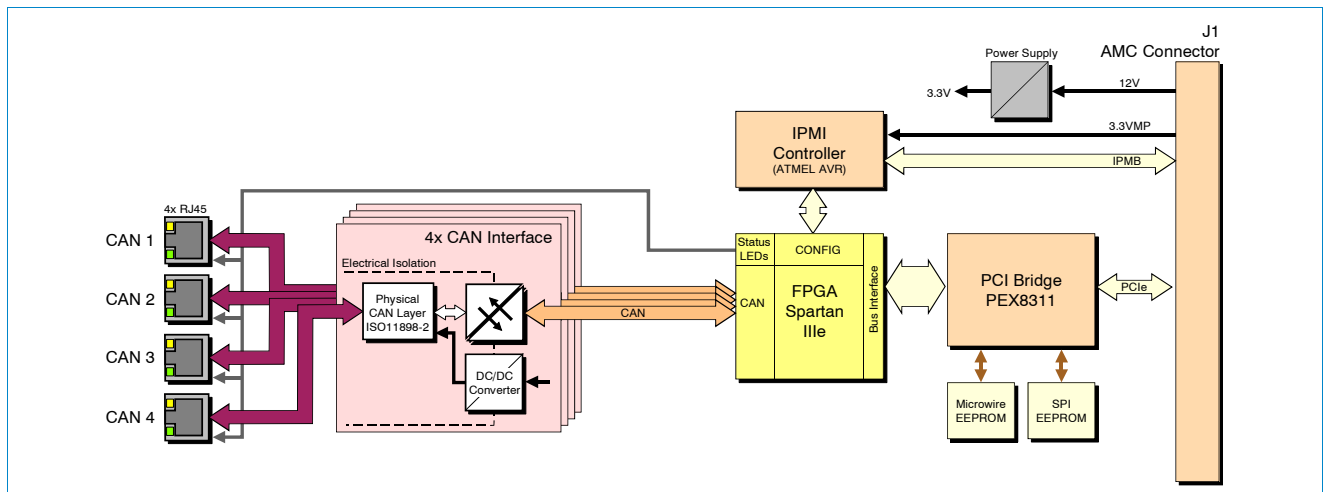
The four independent CAN nets according to ISO 11898-1 are driven by the esd Advanced CAN Core (esdACC) CAN controller implemented in the Xilinx Spartan 3e FPGA.

Controlled by the FPGA the AMC-CAN4 supports PCI bus mastering as an initiator, meaning that it is capable of initiating write cycles to the host CPU's RAM independent of the CPU or the system DMA controller. This results in a reduction of overall latency on servicing I/O transactions in particular at higher data rates.



### Software Support

CAN layer 2 (CAN-API) software drivers are available for Windows, RTX, VxWorks<sup>1</sup>, QNX<sup>1</sup> and Linux<sup>1</sup> supporting up to 24 CAN nets. Drivers for other operating systems are available on request. The CANopen<sup>®</sup> software package is available for Windows, VxWorks<sup>1</sup>, RTX<sup>1</sup>, QNX<sup>1</sup> and Linux<sup>1</sup>. The J1939 software package is available for Windows, VxWorks<sup>1</sup>, QNX<sup>1</sup> and Linux<sup>1</sup>.



### Technical Specifications:

<b>MicroTCA™/AMC® standards:</b>	
μTCA:	PICMG® MTCA.0 R1.0, PICMG® AMC.0 R2.0
IPMI:	IPMI V1.5, controller Atmel® AVR
Updates:	PICMG® HPM.1 R1.0
PCIe bridge:	PCISIG® PCIe spec. R.1.0a
<b>CAN interfaces:</b>	
CAN controller:	esdACC in FPGA Spartan® 3e, acc. to ISO 11898-1 (CAN 2.0 A/B)
Physical interface:	4x CAN high-speed interface acc. to ISO 11898-2, electrically isolated, bit rate up to 1 Mbit/s
CAN connector:	4x RJ45, pin assignment acc. to CiA DR303-1
<b>General :</b>	
Dimensions:	mid-height, single-width (73.5 x 180 mm) AMC
Ambient temp.:	0 ... +70 °C (free convection)
Humidity:	max. 90 %, non-condensing

<b>General (continued):</b>	
Power supply:	3.3 V ( $I_{3.3VMPMAX} = 70 \text{ mA}$ ), 12 V ( $I_{12VTYPICAL} = 0.4 \text{ A}$ , $I_{12VMAX} = 0.5 \text{ A}$ )
Connectors:	J1: AMC B/B+ compatible (MicroTCA™)
LEDs:	blue (hot plug), red (IPMI), green (OK), 4x yellow and 4x green (CAN status)
<b>Order information:</b>	
Designation	order no.
AMC-CAN4	4x CAN interface, acc to ISO11898-2 U.1002.01
AMC-CAN-RJ45-DSUB9 cable	Adapter cable RJ45 male to 9-pin DSUB male connector, length 1.5 m U.1002.10
CAN-DRV-LCD	Object licence for Windows and Linux incl. CD-ROM C.1101.02

<sup>1</sup> For detailed information about the driver availability of your special operating system please contact our sales team.

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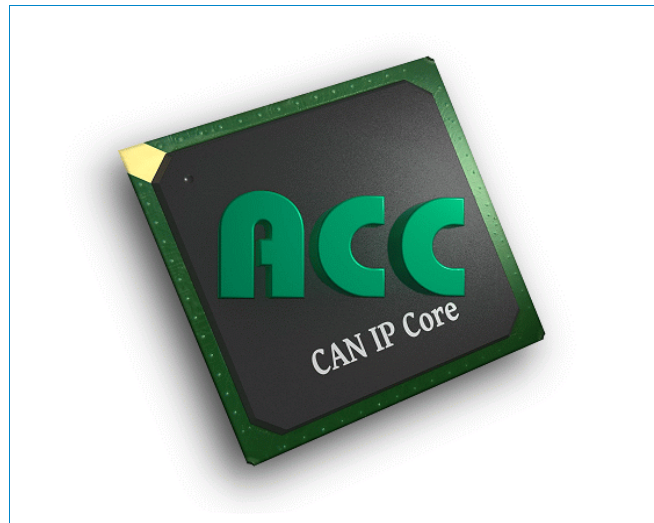
## Driven by esdACC (Advanced CAN Core)

### Basic Product Features:

- CAN ISO 11898-1 protocol compatibility
- 11-bit and 29-bit CAN IDs
- Bit rates from 10kbit/s up to 1 Mbit/s supported
- Receive buffer (64 CAN messages)
- Complete access to CAN error counters
- Programmable error warning limit
- Error code capture register
- Error interrupt for each CAN bus error
- Arbitration lost interrupt with detailed bit position
- Single-shot transmission (no re-transmission)
- Listen only mode (no acknowledge, no active error flags)
- Automatic bit rate detection (software supported bit rate detection)
- Acceptance filter (4-byte code, 4-byte mask)
- Self reception mode (reception of 'own' messages)

### Superior esdACC Features:

- Operating system independently programmable via esd's NTCAN-API
- 32-bit register interface optimized for CAN needs
  - Easy to program
  - Transmission and reception of CAN frames with a minimum of register accesses
- RX and TX timestamping (64-bit wide, bit accurate, resolution may vary with input clock, in any case  $\leq 62.5$  ns, usually 20.833 ns)
  - On hardware with IRIG-B interfaces IRIG-B time is used for timestamping
- TX FIFO (8 CAN frames deep)
  - Providing the means to generate 100% busload even with non-realtime operating systems
  - Providing the means for real back-to-back transmission
- Frame accurate abortion of transmissions with minimum delay
  - e.g. for driver timeouts
  - ISO11898-1 conform
  - Aborted frames in FIFO won't be blocked by low priority TX
- Hardware timer to provide accurate software timeouts beyond operating system accuracy
- Bus mastering in RX direction takes the load off host CPU (needs bus master capable local bus to host interface)
- Optional integration with 32-Bit microcontroller to further relieve host CPU
- Optional different sources for timestamps (e.g. IRIG-B)
- Using FPGA technology provides the option to tailor any feature to any customer's needs, including optional integration with customer's FPGA content
- CAN error injection units
  - Simulating a wide range of error situations on CAN bus, e.g.:
    - ID pollution (100% bus load on certain CAN ID/priority)
    - Defective sensor (Destroying all CAN messages of a given CAN ID)
  - Different trigger modes
    - Bit pattern match
    - Time triggered
    - Immediate regarding CAN arbitration
    - External
  - 'Cross CAN bus triggering' (event on one CAN bus triggers event on another bus)



### Driver Availability:

Windows, Linux, QNX<sup>1</sup>, VxWorks<sup>1</sup>, RTX<sup>1</sup>

<sup>1</sup> For detailed information about the driver availability of your special operating system please contact our sales team.

### Available higher level protocols:

CANopen, ARINC825, J1939

For further information on the esdACC IP Core please contact our sales team.